300KHz, 5A/3A, 26V High-Efficiency Synchronous-Rectified Buck Converter

General Description

The uP6306 is a high efficiency synchronous-rectified buck converter with internal power switches. Fixed 300kHz PWM operation allows possible smallest output ripple and external component size. With high conversion efficiency and small package, the uP6306 is ideally suitable for applications where PCB area is especially concerned.

Designed with slope-compensated current mode control, the uP6306 features fast transient response to step load change. The converter supports PSM mode operation at light load condition, thus yields very high efficiency over a wide range of load current.

With integrated high voltage MOSFET, the uP6306 is capable of delivering 5A/3A output current over a wide input range from 5V to 26V. The output voltage is adjustable from 0.8V to 80% of V_{IN} by a voltage divider.

Other features include internal soft-start, chip enable, under-voltage, over-temperature and over-current protections. The uP6306 is available in a thermally enhanced PSOP-8 package.

Applications

- **Distributed Power Systems**
- **Networking Systems**
- **FPGA/DSP/ASIC Power Supplies**
- **Green Electronics/ Appliances**
- **Notebook Computers**

Features

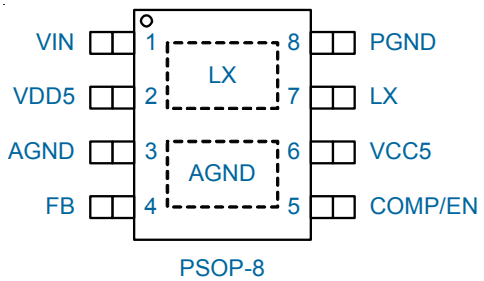
- **5V to 26V Input Voltage Range**
- **Integrated Power MOSFET**
  - **60mΩ(5A)/120mΩ(3A) PMOSFET for High Side Switch**
  - **30mΩ(5A)/60mΩ(3A) NMOSFET for Low Side Switch**
- **Automatic PWM/PSM Operation for High Efficiency**
- **Up to 96% Conversion Efficiency**
- **Accurate Reference: 0.8V (+/- 1.5%)**
- **Current Mode PWM Operation**
- **Fixed Frequency: 300kHz**
- **Internal Soft-Start**
- **Under-Voltage Protection**
- **Over-Temperature and Over-Current Protection**
- **PSOP-8 Package**
- **RoHS Compliant and Halogen Free**

Ordering Information

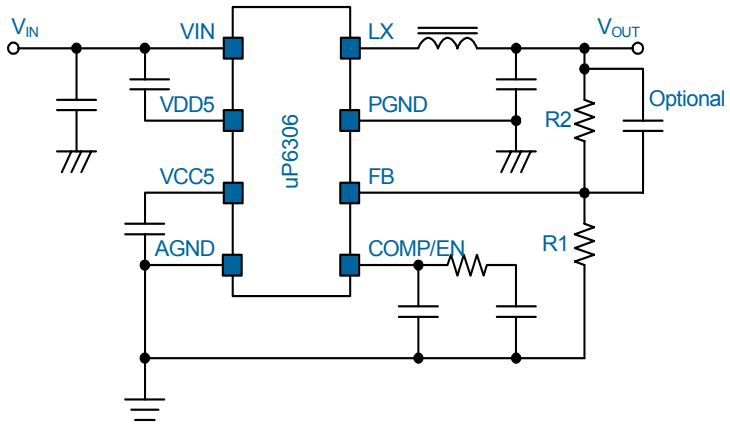
Order Number	Package Type	Remark
uP6306NSM8-XX	PSOP - 8L	NIKO MOSFETS
uP6306USM8-XX	PSOP - 8L	UBIQ MOSFETS
Code XX : Operation Current e.g.: 03 = 3A; 05 = 5A		

Note: uPI products are compatible with the current IPC/ JEDEC J-STD-020 requirement. They are halogen-free, RoHS compliant and 100% matte tin (Sn) plating that are suitable for use in SnPb or Pb-free soldering processes.

Pin Configuration & Typical Application Circuit



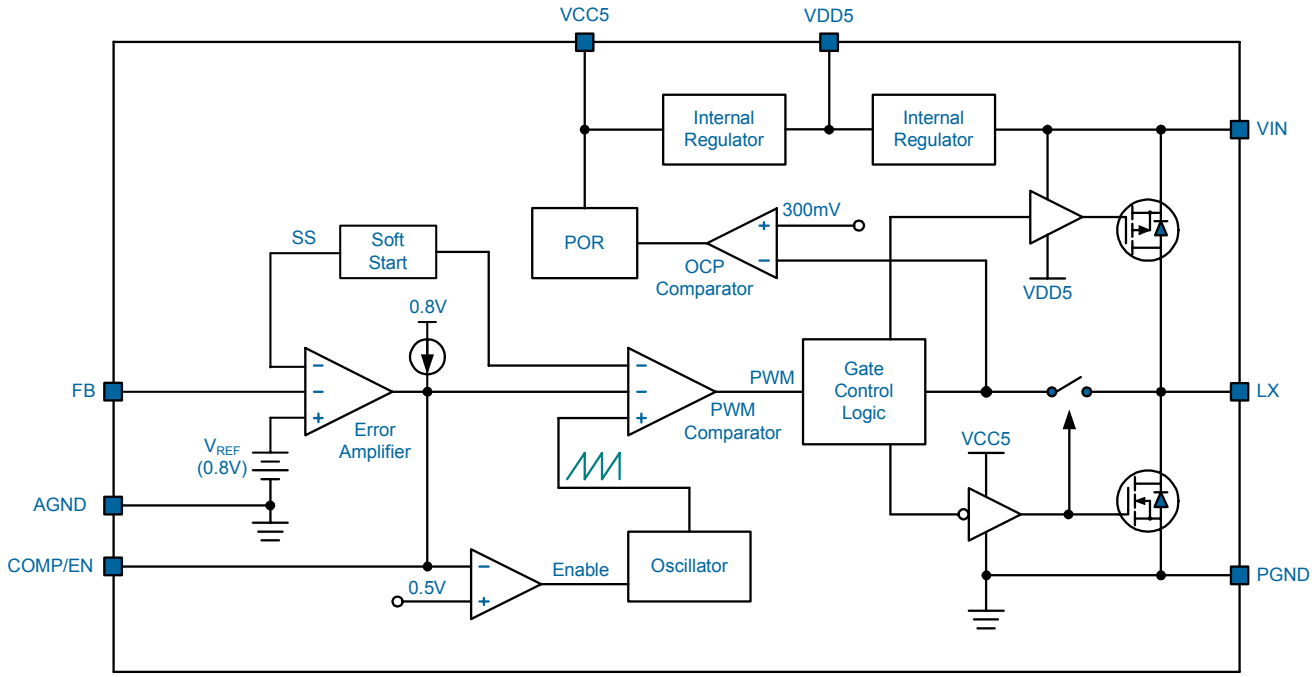
PSOP-8



Functional Pin Description

Pin No.	Pin Name	Pin Function
1	VIN	**Power Supply Input.** Input voltage that supplies current to the output voltage and powers the internal 5V linear regulators.
2	VDD5	**Bias Supply for Upper MOSFET Driver.** Connect a minimum 4.7uF ceramic capacitor from this pin to VIN pin to bypass the bias voltage.
3	AGND	**Signal Ground.** Connect the return of all small signal components to this pin.
4	FB	**Feedback Voltage.** This pin is the inverting input to the error amplifier. A resistor divider from the output to AGND is used to set the regulation voltage.
5	COMP/EN	**Error Amplifier Output.** This is the output of the error amplifier (EA) and the non-inverting input of the PWM comparators. Use this pin in combination with the FB pin to compensate the voltage-control feedback loop of the converter.
6	VCC5	**Bias Supply.** This pin is the output of internal 5V linear regulator, supplying current for the lower MOSFET driver and internal circuitry. Connect a minimum 4.7uF ceramic capacitor form this pin to AGND pin to bypass the bias voltage.
7	LX	**Internal Switches Output.** Connect this pin to the output inductor.
8	PGND	**Main Power Ground Return.** Connect to the output and input capacitor return.
Exposed Pad I		**Internal Switches Output.** The exposed pad should be well soldered to PCB with multiple vias to ground plane for optimal thermal performance. This pin should be electrically connected to LX pin on PCB.
Exposed Pad II		**Signal Ground.** Connect the return of all small signal components to this pin.

Functional Block Diagram



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Designed with current mode control, the uP6306 features fast transient response to step load change. The converter supports PSM mode operation at light load condition, thus yields very high efficiency over a wide range of load current.

With integrated high voltage MOSFET, the uP6306 is capable of delivering 5A/3A output current over a wide input range from 5V to 26V. The output voltage is adjustable from 0.8V to 80% of V_{IN} by a voltage divider. Other features include internal soft-start, chip enable, under-voltage, over-temperature and over-current protections. The uP6306 is available in a thermally enhanced PSOP-8 package.

Input Supply Voltage, V_{IN}

The uP6306 operates with single supply input at VIN pin. The VIN pin supplies current for output voltages and provides current for internal control circuit and gate drivers. The supply voltage range is from 5V to 26V. The uP6306 draws pulsed current from VIN pin with sharp edges each time the upper switch turns on, resulting in voltage ripples and spikes at supply input. A minimum 22uF ceramic capacitor with shortest PCB trace is highly recommended for bypassing the supply input.

The uP6306 integrates two 5V linear regulators. A linear regulator regulates (VIN - VDD5) voltage at 5V for upper gate driver. The other linear regulator regulates (VCC5 - GND) voltage at 5V for internal control circuit and lower gate driver. Both VDD5 and VCC5 need a minimum 4.7uF capacitor for locally bypassing the output voltage of linear regulators.

The VCC5 voltage is continuously monitored for power on reset (POR) to insure its voltage is high enough for normal operation. The POR threshold level is typically 4.2V at VCC5 rising. For fixed V_{IN} = 5V operation, connect VCC5 pin to VIN pin directly. Otherwise the dropout voltage of the linear regulator will make VCC5 < 4.2V and below its POR threshold voltage.

Power Switches

The uP6306 integrates internal power switches to form a synchronous buck converter: 60mΩ(5A)/120mΩ(3A) PMOSFET for upper switches 30mΩ(5A)/60mΩ(3A) NMOSFET for lower switch. The source of PMOSFET is connected to VIN pin, the source of NMOSFET is connected to PGND pin. The drains of both MOSFETs are connected together to LX pin.

Bias Voltage

Internal linear regulators generate voltages for driving the power MOSFET and biasing the internal control circuits. The VDD5 voltage is regulated to -5V with respect to VIN fro driving the PMOSFET. The gate of PMOSFET is driven to VDD5 when turned on. A minimum 4.7uF ceramic capacitor is required from VDD5 to VIN pin for locally bypassing the VDD5 voltage.

The VCC5 is regulated to +5V with respective to AGND pin for driving the NMOSFET and biasing the internal control circuits. The gate of NMOSFET is driven to VCC5 when turned on. A minimum 4.7uF ceramic capacitor is required from VCC5 to AGND pin for locally bypassing the VCC5 voltage.

Chip Enable

The COMP/EN is a multifunctional pin: control loop compensation and chip enable as shown in Figure 1. An Enable Comparator monitors the COMP/EN pin for chip enable. A signal level transistor is adequate to pull this pin down to ground and shut down the uP6306. An 80uA current source charges the external compensation network with 0.8V ceiling when this pin is released. If the voltage at COMP/EN pin exceeds 0.5V, the uP6306 initiates its softstart cycle.

The 80uA current source keeps charging the COMP/EN pin to its ceiling until the feedback loop boosts the COMP/EN pin higher than 0.8V according to the feedback signal. The current source is cut off when V_{COMP} is higher than 0.8V during normal operation.

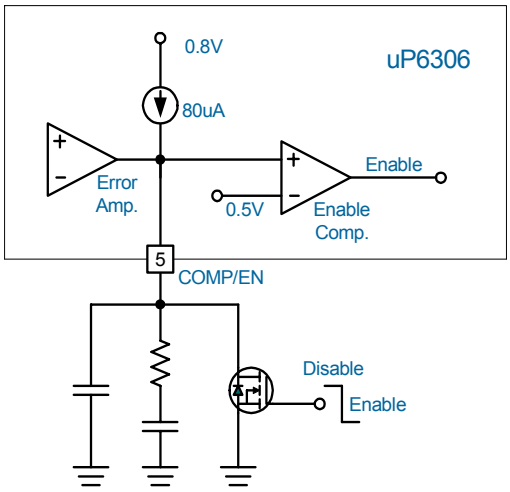


Figure 1. Chip Enable Function

Functional Description

SoftStart

A built-in Soft Start is used to prevent surge current from power supply input during turn on (referring to the Functional Block Diagram). The error amplifier is a three-input device. Reference voltage V_{REF} or the internal soft start voltage SS whichever is smaller dominates the behavior of the non-inverting inputs of the error amplifier. SS internally ramps up to 0.8V in 2ms after the softstart cycle is initiated. The ramp is created digitally, so there will be 100 small discrete steps. Accordingly, the output voltage will follow the SS signal and ramp up smoothly to its target level.

The SS signal keeps ramping up after it exceeds the internal 0.8V reference voltage. However, the internal 0.8V reference voltage takes over the behavior of error amplifier after SS > V_{REF}. When the SS signal climb to its ceiling voltage (4V), the uP6306 claims the end of softstart cycle and enable the under voltage protection of the output voltage.

Figure 2 shows a typical start up interval for uP6306 where the COMP/EN pin has been released from a grounded (system shutdown) state.

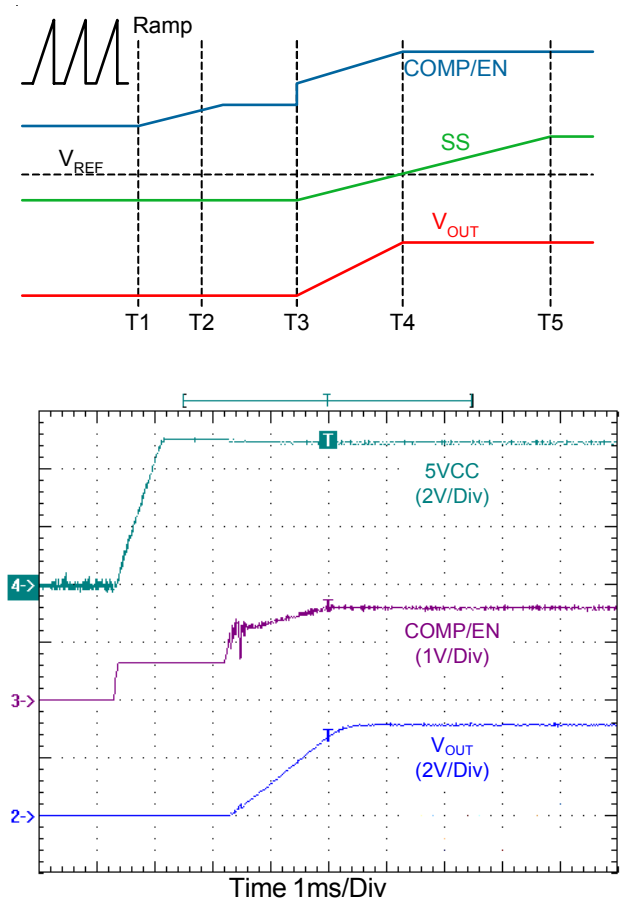


Figure 2. Softstart Behavior.

The internal 80uA current source starts to charge the compensation network after the COMP/EN pin is released from grounded at T1. The COMP/EN exceeds 0.5V and enables the uP6306 at T2. The COMP/EN continues ramping up and stays at 0.8V before the SS starts ramping up at T3. The uP6306 initializes itself such as current limit level setting (see the relative section) during the time interval between T2 and T3. The output voltage follows the internal SS and ramps up to its final level during T3 and T4. At T4, the reference voltage V_{REF} takes over the behavior of the error amplifier as the internal SS crosses V_{REF}. The internal SS keeps ramping up and stay at 4V at T5, where the uP6306 asserts the end of softstart cycle.

PWM Operation

The uP6306 adopts slope-compensated, current mode PWM control capable of achieving 80% duty cycle. During normal operation, the uP6306 operates at PWM mode to regulate output voltage by transferring the power to the output voltage cycle by cycle at a constant 300kHz frequency. The uP6306 turns on the upper switch at each rising edge of the internal oscillator allowing the inductor current to ramp up linearly. The switch remains on until either the current-limit is tripped or the PWM comparator turns off the switch for regulating output voltage. The upper switch current is sensed, slope compensated and compared with the error amplifier output COMP/EN to determine the adequate duty cycle. The FB pin senses output feedback voltage from an external resistive divider.

When the load current increases, it causes a slight decrease in the feedback voltage relative to the 0.8V reference, which in turn, causes the error amplifier output voltage to increase until the average inductor current matches the new load current.

A Pseudo Diode Emulator monitors inductor current by sensing voltage drop across the lower switch when it turns on. The lower switch turns off to emulate the free wheel diode used in traditional asynchronous buck converter and allows the converter entering discontinuous conduction mode when inductor current crosses zero. This reduces conduction loss and increase power conversion efficiency at light condition.

PSM Operation

A finite minimum on-time for both upper and lower switches is implemented for normal operation. Consequently, the converter will enter pulse-skipping mode (PSM) during extreme light load condition or when modulation index (V_{OUT}/ V_{IN}) is extreme low. The equivalent switching frequency is reduced. This could reduce switching loss and further

increase power conversion efficiency. The lower switch turns on with optimal deadtime and picks up the inductor current after the upper switch turns off, allowing the inductor current to ramp down linearly. The switch remains on until the next rising edge of oscillator turns on the upper switch. The uP6306 regulates the output voltage by controlling the ramp up/down duty cycle of inductor current. The high frequency switching ripple is easily smoothed by the output filter.

Current Limit Function

The uP6306 continuously monitors the inductor current for current limit by sensing the voltage drop across the upper switch when it turns on. When the inductor current is higher than current limit threshold (7A(5A)/4.5A(3A) minimum), the current limit function activates and forces the upper switch turning off to limit inductor current cycle by cycle. If the load continuously demands more current than what uP6306 could provide, uP6306 can not regulate the output voltage. Eventually under voltage protection will be triggered and shuts down the uP6306 if V_{OUT} is too low.

Undervoltage Protection

Undervoltage Protection is triggered if the FB voltage is lower than 0.4V and shuts down uP6306. The uP6306 can only be reset by POR of V_{IN} or toggling the COMP/EN pin.

Output Voltage Setting and Feedback Network

The output voltage can be set from V_{REF} to V_{IN} by a voltage divider as:

$$V_{OUT} = \frac{R1+R2}{R1} \times V_{REF}$$

The internal V_{REF} is 0.8V with 1.5% accuracy. In real applications, a 22pF feedforward ceramic capacitor is recommended in parallel with R2 for better transient response.

Absolute Maximum Rating

Supply Input Voltage, V_{IN} (Note 1) ---------- -0.3V to +30V
LX to GND
DC ---------- -0.7V to (V_{IN} + 0.3V)
< 200ns ---------- -5V to 40V
VDD to VIN ---------- -6V to +0.3V
Other Pins ---------- -0.3V to +6V
Storage Temperature Range ---------- -65°C to +150°C
Junction Temperature ---------- 150°C
Lead Temperature (Soldering, 10 sec) ---------- 260°C
ESD Rating (Note 2)
HBM (Human Body Mode) ---------- 2kV
MM (Machine Mode) ---------- 200V

Thermal Information

Package Thermal Resistance (Note 3)
θ_{JA} PSOP-8 ---------- 50°C/W
θ_{JC} PSOP-8 ---------- 5°C/W
Power Dissipation, P_D @ T_A = 25°C
PSOP-8 ---------- 2W

Recommended Operation Conditions

Operating Junction Temperature Range (Note 4) ---------- -40°C to +125°C
Operating Ambient Temperature Range ---------- -40°C to +85°C
Supply Input Voltage, V_{IN} ---------- +5V to 26V

Electrical Characteristics

(V_{IN} = 12V, T_A = 25°C, unless otherwise specified)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Units
Supply Input						
Supply Voltage	V_{IN}		5	--	26	V
Quiescent Supply Current	I_{IN_Q}	V_{OUT} = 5V, I_{OUT} = 0A	--	0.9	--	mA
Shutdown Current	I_{IN_SD}	COMP/EN = 0V, V_{OUT} = 0V	--	50	70	uA
POR Threshold	V_{CC5RTH}	V_{CC5} rising	--	4.2	4.5	V
POR Hysteresis	V_{CC5HYS}		--	0.2	--	V
Bias Supply						
VCC5	V_{CC5}	COMP/EN = 0.6V	4.8	5.0	5.2	V
V_{IN} - VDD5	V_{DD5}	COMP/EN = 0.6V	4.7	5.0	5.3	V

Electrical Characteristics

Parameter	Symbol	Test Conditions	Min	Typ	Max	Units
Oscillator						
Free Running Frequency	f_{OSC}		255	300	345	kHz
Ramp Amplitude	ΔV_{RAMP}	V_{IN} = 12V	--	1.12	--	V
Maximum Duty Cycle			73	78	83	%
Minimum On Time		V_{OUT} = 1.6V	--	400	--	ns
Reference Voltage						
Nominal Feedback Voltage	V_{FB}		0.79	0.80	0.81	V
Error Amplifier						
Open Loop DC Gain	AO	Guaranteed by Design	70	80	--	dB
Gain-Bandwidth Product	GBW	Guaranteed by Design	--	30	--	MHz
Transconductance			--	200	--	uS
Output Source Current		V_{FB} < V_{REF}	24	32	--	uA
Output Sink Current		V_{FB} > V_{REF}	24	32	--	uA
Chip Disable Threshold		COMP/EN falling	--	0.5	--	V
COMP/EN Pull-High Current		COMP/EN = 0V	--	2	5	uA
Power Switches						
Upper Switch On Resistance	$R_{DS(ON)}$	Operation Current = 5A	--	60	--	mΩ
		Operation Current = 3A	--	120	--	mΩ
Lower Switch On Resistance	$R_{DS(ON)}$	Operation Current = 5A	--	30	--	mΩ
		Operation Current = 3A	--	60	--	mΩ
Lower Switch Current Limit		Operation Current = 5A	7	--	10	A
		Operation Current = 3A	4.5	--	7.5	A
Protection						
Output Under Voltage Protection	V_{FB_UVP}	V_{FB} falling	--	0.4	--	V
Over Temperature Protection			--	150	--	°C

Note 1. Stresses listed as the above "Absolute Maximum Ratings" may cause permanent damage to the device. These are for stress ratings. Functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may remain possibility to affect device reliability.

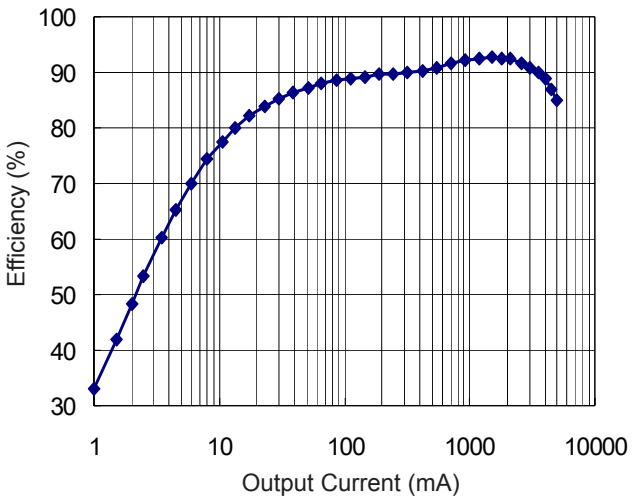
Note 2. Devices are ESD sensitive. Handling precaution recommended.

Note 3. θ_{JA} is measured in the natural convection at T_A = 25°C on a low effective thermal conductivity test board of JEDEC 51-3 thermal measurement standard.

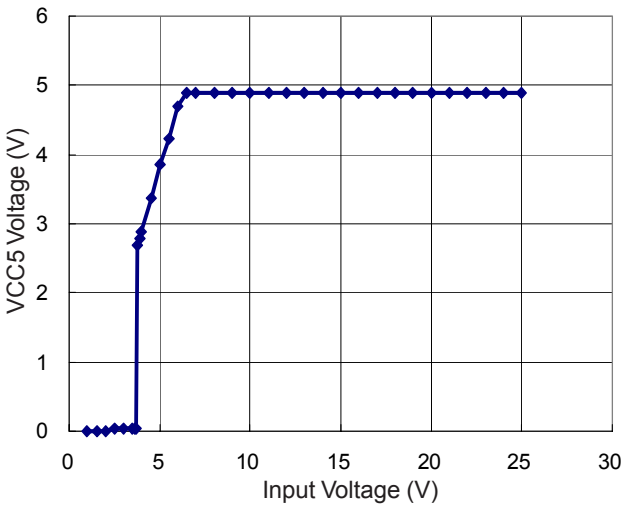
Note 4. The device is not guaranteed to function outside its operating conditions.

Typical Operation Characteristics

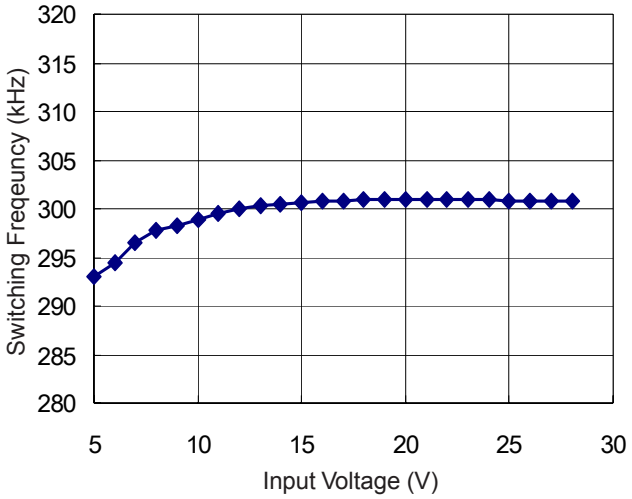
Efficiency vs. Output Current



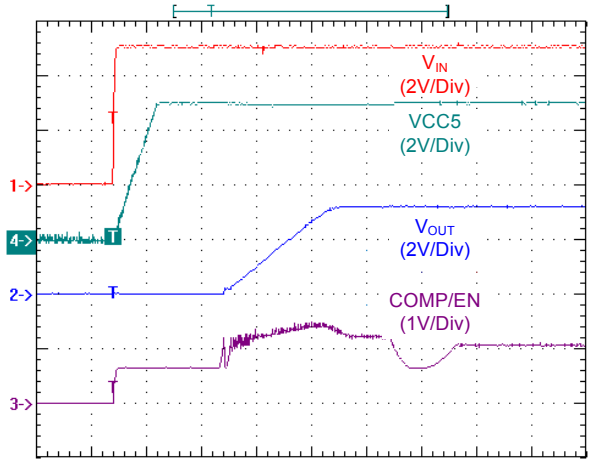
VCC5 Voltage Line Regulation



Switching Frequency vs. Input Voltage

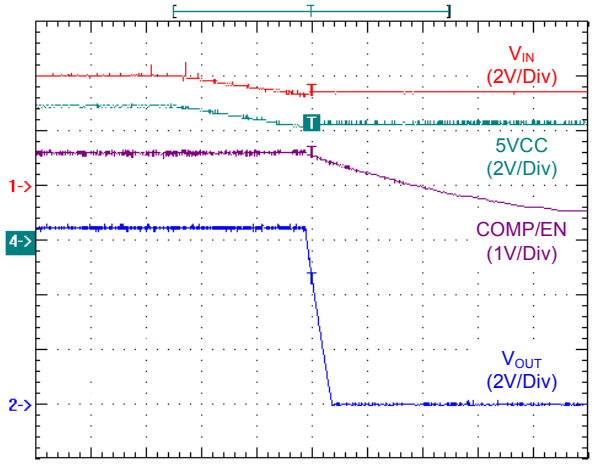


Power On Waveforms



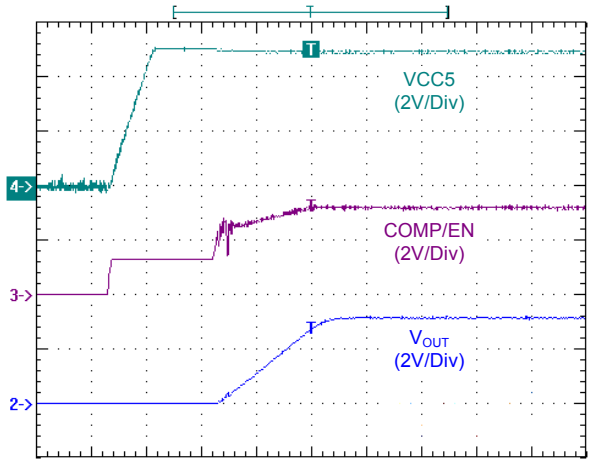
Time (1ms/Div)
V_{IN} = 5V, V_{OUT} = 3.3V, I_{OUT} = 1A.

Power Off Wavefroms



Time (1ms/Div)
V_{IN} = 5V, V_{OUT} = 3.3V, I_{OUT} = 1A.

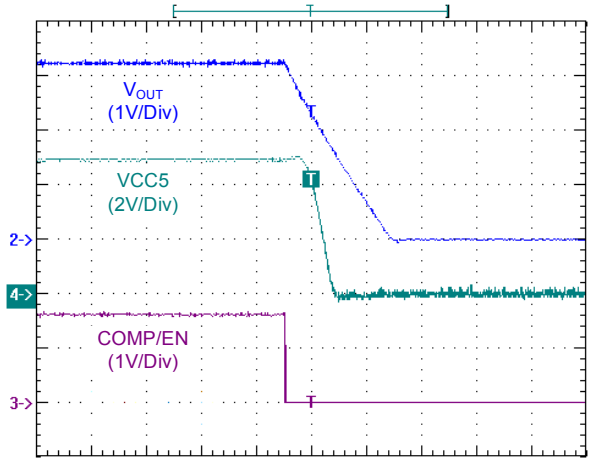
Turn On Waveforms



Time (1ms/Div)
V_{IN} = 5V, V_{OUT} = 3.3V, I_{OUT} = 1A.

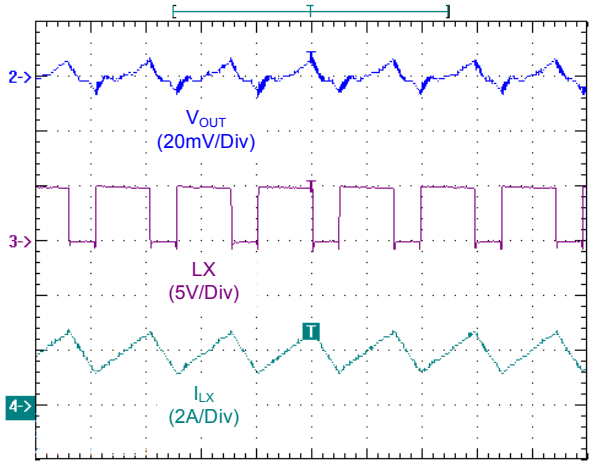
Typical Operation Characteristics

Turn Off Waveforms



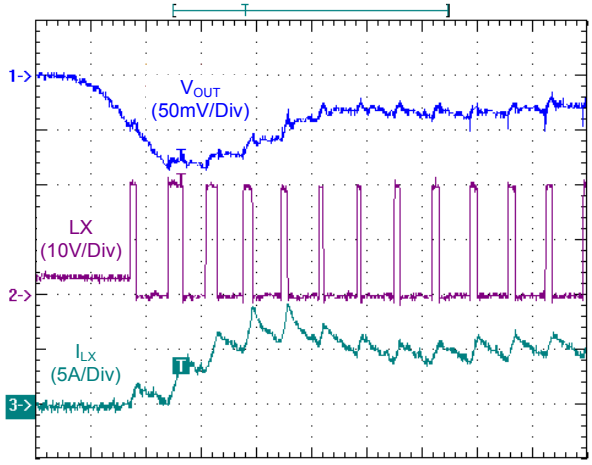
Time (250us/Div)
V_{IN} = 5V, V_{OUT} = 3.3V, I_{OUT} = 1A.

Steady State Operation



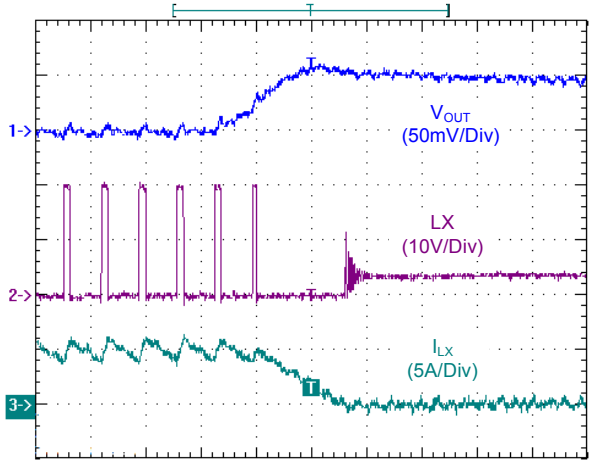
Time (2.5us/Div)
V_{IN} = 5V, V_{OUT} = 3.3V, I_{OUT} = 2A.

Load Transient Response



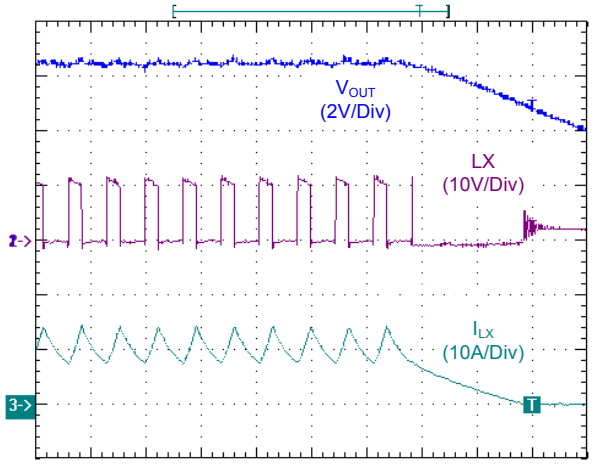
Time (5us/Div)
V_{IN} = 20V, V_{OUT} = 3.3V, I_{OUT} = 0 to 5A.

Load Transient Response



Time (5us/Div)
V_{IN} = 20V, V_{OUT} = 3.3V, I_{OUT} = 5 to 0A.

Over Current Protection



Time (5us/Div)
V_{IN} = 12V, V_{OUT} = 3.3V.

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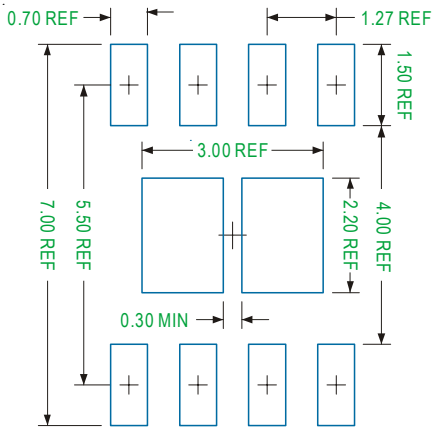
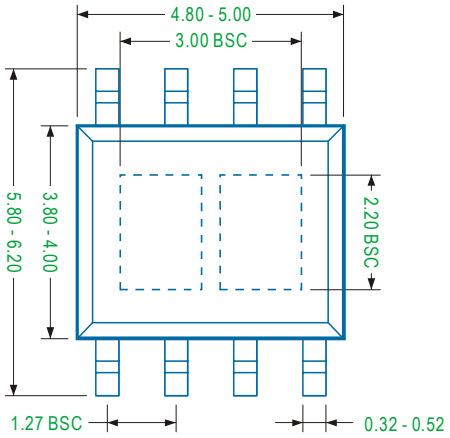
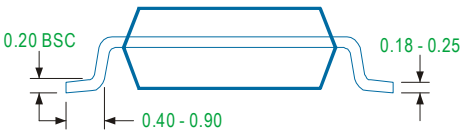
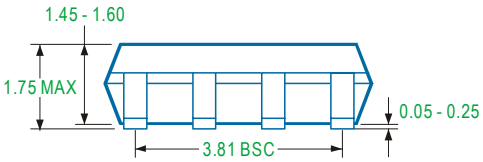
Package Information



Recommended Solder Pad Layout







Note

1. Package Outline Unit Description:
   BSC: Basic. Represents theoretical exact dimension or dimension target
   MIN: Minimum dimension specified.
   MAX: Maximum dimension specified.
   REF: Reference. Represents dimension for reference use only. This value is not a device specification.
   TYP. Typical. Provided as a general value. This value is not a device specification.
2. Dimensions in Millimeters.
3. Drawing not to scale.
4. These dimensions do not include mold flash or protrusions. Mold flash or protrusions shell not exceed 0.15mm.